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Code : 041402

B.Tech. 4th Semester Exam., 2014

DIGITAL ELECTRONICS

Time : 3 hours

Full Marks : 70

Instructions:

- (i) The marks are indicated in the right-hand margin.
- (ii) There are **NINE** questions in this paper.
- (iii) Attempt **FIVE** questions in all.
- (iv) Question No. 1 is compulsory.

1. Choose the correct option from the following
(any seven) : $2 \times 7 = 14$

(a) A quantity having continuous wave is

- (i) a digital quantity
- (ii) an analog quantity
- (iii) a binary quantity
- (iv) a natural quantity

(b) The sum of 11010 + 01111 equals

- (i) 101001
- (ii) 101010
- (iii) 110101
- (iv) 101000

$$\begin{array}{r} 11010 \\ + 01111 \\ \hline 00101 \end{array}$$

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(Turn Over)

(c) The output of a gate is low if and only if its input are HIGH. It is true for

- (i) AND
- (ii) XNOR
- (iii) NOR
- (iv) NAND

(d) An example of a standard SOP expression is

- (i) $\overline{A}\overline{B} + \overline{A}BC + \overline{A}BD$
- (ii) $\overline{A}BC + ACD$
- (iii) $\overline{A}B + \overline{A}B + AB$
- (iv) $AB\overline{C}D + \overline{A}B + \overline{A}$

(e) To implement the expression of $\overline{A}BCD + \overline{A}\overline{B}CD + \overline{A}B\overline{C}D$, it takes one OR gate and

- (i) one AND gate
- (ii) three AND gates
- (iii) three AND gates and four inverters
- (iv) three AND gates and three inverters

(f) The invalid state of an S-R latch occurs when

- (i) $S = 1, R = 0$
- (ii) $S = 0, R = 1$
- (iii) $S = 1, R = 1$
- (iv) $S = 0, R = 0$

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(Continued)

(g) The device used to convert a binary number to a 7-segment display format is

- (i) multiplexer
- (ii) encoder
- (iii) decoder
- (iv) register

(h) An asynchronous counter differs from a synchronous counter in

- (i) the number of states in its sequence
- (ii) the method of clocking
- (iii) the type of flip-flop used
- (iv) the value of the modulus

(i) A stage in a shift register consists of

- (i) a latch
- (ii) a flip-flop
- (iii) a byte of storage
- (iv) four bits of storage

(j) A 32-bit data word consists of

- (i) 2 bytes
- (ii) 4 nibbles
- (iii) 4 bytes
- (iv) 3 bits and 1 nibble

(Turn Over)

2. (a) Make a K-map for the function

$$F = A\bar{B} + AC + A\bar{D} + AB + ABC$$

5

(b) Express F , in standard SOP and POS form.

5

(c) Minimize \bar{F} and realize the minimal expression using NOR gate only.

4

3. (a) Prove the following algebraically :

$$2\frac{1}{2} + 2\frac{1}{2} = 5$$

(i) $(A+B)(A+\bar{B}) = A \oplus B$

(ii) $(A+B)(A+\bar{B})(\bar{A}+B) = AB$

(b) Convert decimal number 75 into Grey code.

4

(c) Verify a two-level AND-OR gate is equivalent to NAND-NAND.

5

4. (a) Draw a circuit diagram of an RTLEX-OR gate. Explain its operation.

7

(b) Draw a circuit diagram of DTL gate and explain it. What are fan-in and fan-out? How will you increase the fan-out of the gate?

7

(5)

5. (a) Design a full adder using only NAND gate. 7
- (b) Design a 8 to 1 line multiplexer using 4 to 1 line multiplexer. 7
6. (a) Differentiate between synchronous and asynchronous counter. 7
- (b) Design a 4-bit synchronous up counter. 7
7. (a) Explain the following flip-flops with their diagrams and truth tables : 7
- (i) SR F/F
- (ii) J-K F/F
- (iii) D F/F
- (iv) T F/F
- (b) Design D F/F from J-K F/F. 7
8. (a) Explain the working principle of a successive approximation ADC with the help of circuit diagram. 7
- (b) Find the output voltage from a 5-bit ladder D/A converter which has a digital input of 11010. Assume 0 = 0 V and 1 = +10 V. 7

(6)

9. Write short notes on any two of the following : 7×2=14
- (a) Data transfer in a shift register
- (b) ROM
- (c) Astable multivibrator using 555
- (d) Digital comparator
