Code : 041301

B.Tech 3rd Semester Exam., 2015

BASIC ELECTRONICS

Time : 3 hours   Full Marks : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are **NINE** questions in this paper.

(iii) Attempt **FIVE** questions in all.

(iv) Question No. **1** is compulsory.

1. Answer the following questions :   2×7=14

   (a) Why is silicon preferred over germanium in making of semiconductor devices?

   (b) What do you understand by transition capacitance of a diode?

   (c) Why we cannot measure the barrier potential of a diode using voltmeter?

   (d) Explain one disadvantage of bridge rectifier.

   (e) Capacitor filter is not suited for heavy loads. Why?

2. (a) Derive and explain an intrinsic carrier concentration (n_i) of a semiconductor.

   (b) Explain the operation and characteristics of light emitting diode.   6+8=14

3. (a) For the circuit shown in Figure 1, determine

   (i)   d.c. output voltage

   (ii)   rectification efficiency

   (iii) peak inverse voltage

   (iv)   output frequency

Figure 1
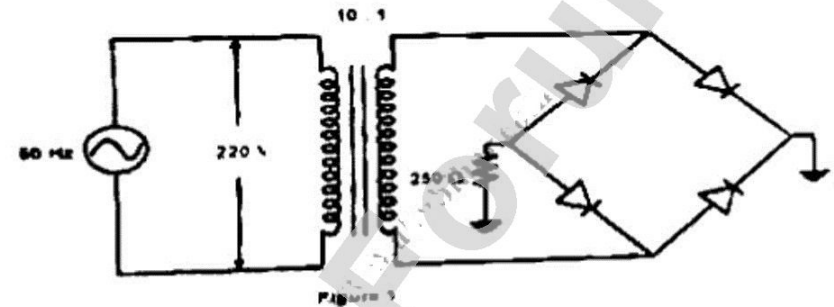
   (b) Explain the operation of p–n silicon diode at equilibrium condition. Also derive the expression for the following :

   (i)   Maximum electric field (E_{max})

   (ii)   Depletion width (W)

   (iii) Built-in potential (V_{bi})   8+6=14

4. (a) Accurately analyze the collector-to-base bias circuit is shown in Figure 2 to determine the I_B, I_C and V_{CE} when

   (i) $\beta = 50$ and

Code : 041301   2

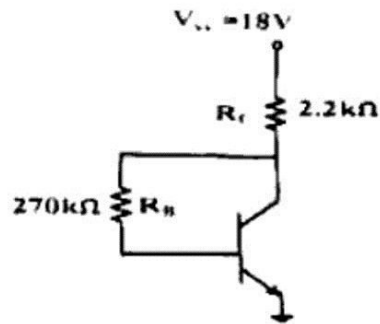(ii) $\beta = 200$ Assume $V_{BE} = 0.7$ V.

Figure 2

(b) Sketch typical BJT common-emitter input and output characteristics. Explain the shapes of the characteristics.   8+6=14

5. (a) Draw the two biasing circuits for JFET and explain.

(b) Derive the gain expression of an integrator and a differentiator using op-amp.   8+6=14

6. (a) Explain the basic operation and characteristics of n-channel depletion type MOSFET.

(b) Sketch a 180° phase control for an SCR. Draw the load waveform and explain the circuit operation.

     8+6=14

7. (a) Draw Sketches to show the basic construction and equivalent circuit of a unijunction transistor (UJT). Briefly explain the device operation.

(b) Design a clamper to perform the function shown in the Figure 3 shown below   8+6=14
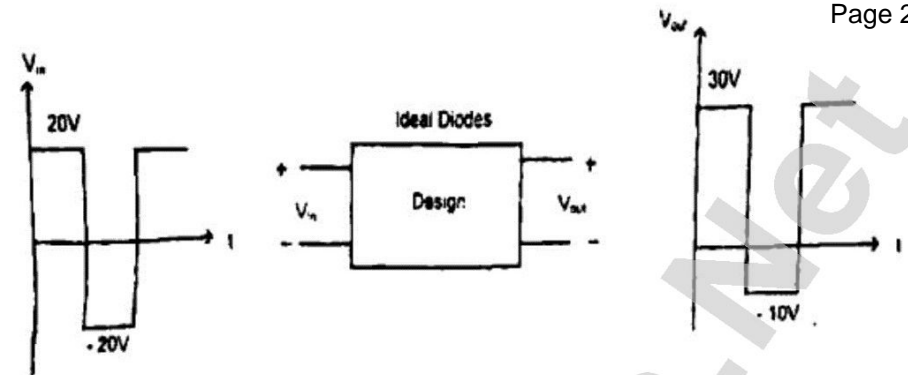
Code : 041301   3   P.T.O.

Figure 3

8. (a) Briefly explain the small signal model of JFET.

(b) An integrator using op-amp has following component values. $R_i = 1k\Omega$, $R_f = 100k\Omega$ and $C_i = 0.1\mu F$. A 1kHz square wave applied to integrator. The amplifier uses ± 15 V supply and output saturates at $\pm 14V$ if input alternates between ± 5 V then.   14

(i)   Determine the maximum change in output

(ii)   Determine the maximum slew rate.

     8+6=14

9. (a) Define the gate power dissipation and explain its importance in SCR.

(b) Explain the operation of centre tapped full wave rectifier. And calculate the rms load current and voltage for a sinusoidal input.   7+7=14

* * *

Code : 041301   4