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for

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ELECTRICAL ENGINEERING

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A WORD TO THE STUDENTS.



Er. R.K. Rajesh
(DIRECTOR)

GATE and Engineering Services Examinations are the most prestigious competitive examinations conducted for graduate engineers. Over the past few years, they have become more competitive as more and more numbers of aspirants are increasingly becoming interested in post graduate qualifications & government jobs for a secured and bright career.

This Formula Book consists of well-illustrated concepts, important formulae and diagrams, which will be highly beneficial at the last leg of candidate's preparation.

It includes all the subjects of Electrical Engineering, Instrumentation Engineering, which are required for all type of competitive examinations. Adequate emphasis has been laid down to all the major topics in the form of Tips / Notes, which will be highly lucrative for objective and short answer type questions.

Proper strategy and revision is a mandatory requirement for clearing any competitive examination. This book covers short notes and formulae for Electronics & Communication Engineering. This book will help in quick revision before the GATE, IES & all other PSUs.

With best wishes for future career

R. K. Rajesh

Director

Engineers Institute of India

eii.rkrajesh@gmail.com

**This book is dedicated to all
Electrical Engineers
Preparing for GATE, IES, SSC& Public sector
examinations.**

Shared on www.EEForum.Net

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Why IES?

Indian engineering services (IES) constitute of engineers that work under the govt. of India to manage a large segment of public sector economy which constitutes of Railroads, Public works, Power, Telecommunications, etc. IES remain the most sought-after careers for the engineering graduates in India. A combined competitive examination is conducted by UPSC for recruitment to the Indian Engineering Services. The exam constitutes of a written exam followed by an interview for personality test.

Why GATE?

In the present competitive scenario, where there is mushrooming of universities and engineering colleges, the only yardstick to measure and test the calibre of engineering students is the GATE.

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Many public sector undertakings such as BHEL, IOCL, NTPC, BPCL, HPCL, BARC and many more PSUs are using the GATE score for selecting candidates for their organizations. Students who qualify in GATE are entitled to a stipend of Rs 8,000 per month during their M.Tech. course. Better remuneration is being offered for students of M.Tech./ME as compared to those pursuing B.Tech/B.E. A good rank assures a good job. After joining M.Tech. at IITs and IISc, one can look at a salary package ranging from Rs 7lakh to 30lakh per annum depending upon specialization and performance. Clearing GATE is also an eligibility clause for the award of JRF in CSIR Laboratories.

Proper strategy and revision is a mandatory requirement for clearing any competitive examination. This book covers short notes and formulae for Electronics & Communication Engineering. This book will help in quick revision before the GATE, IES & all other PSUs.

1

NETWORK THEORY

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1. NETWORK BASICS

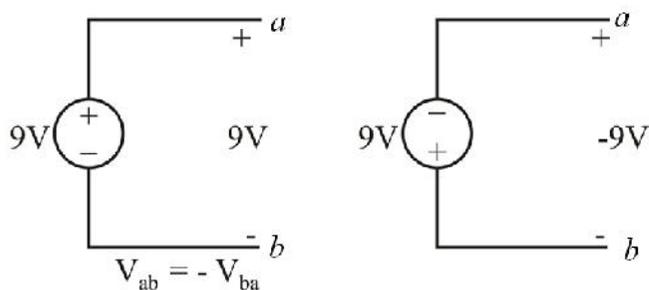
Current: Electric current is the time rate of change of charge flow.

$$i = \frac{dq}{dt} \quad (\text{Ampere})$$

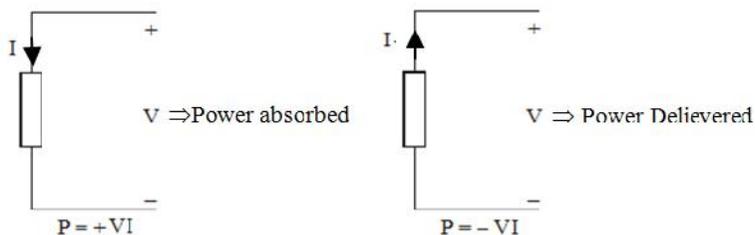
Charge transferred between time t_o and t $q = \int_{t_o}^t i dt$

Sign Convention: A negative current of $-5A$ flowing in one direction is same as a current of $+5A$ in opposite direction.

Voltage: Voltage or potential difference is the energy required to move a unit charge through an element, measured in volts.



Power: It is time rate of expending or absorbing energy.



- Law of conservation of energy must be obeyed in any electric circuit.
- Algebraic sum of power in a circuit, at any instant of time, must be zero.

$$\text{i.e. } \sum P = 0$$

Circuit Elements:

Resistor: Linear and bilateral (conduct from both direction)

In time domain $V(t) = I(t)R$

In s domain $V(s) = RI(s)$

$$R = \frac{l}{A} \text{ ohm}$$

l = length of conductor, ρ = resistivity, A = area of cross section

- Extension of wire to n times results in increase in resistance: $R' = n^2 R$

- Compression of wire results in decrease in resistance:

$$R' = \frac{R}{n^2}$$

Capacitor: All capacitors are linear and bilateral, except electrolytic capacitor which is unilateral.

Time Domain: $i(t) = \frac{Cdv(t)}{dt}$ $v(t) = \frac{1}{C} \int_{-\infty}^t i(t)dt$

In s-domain: $I(s) = sCV(s)$ $V(s) = \frac{1}{sC} I(s)$

- Capacitor doesn't allow sudden change of voltage, until impulse of current is applied.
- It stores energy in the form of electric field and power dissipation in ideal capacitor is zero.
- Impedance $Z_c = -jX_c \Omega$ & $X_c = \frac{1}{\omega C}$; $X_c \rightarrow$ Capacitive reactance ; $\omega = 2\pi f$

Inductor: Linear and Bilateral element

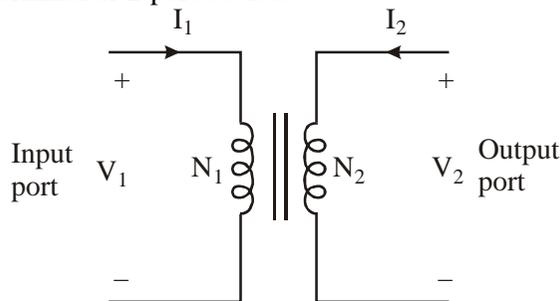
Time Domain: $v(t) = L \frac{di(t)}{dt}$ $i(t) = \frac{1}{L} \int_{-\infty}^t v(t)dt$

Impedance $Z_L = jX_L \Omega$ & $X_L = \omega L \Omega$

In s-domain $V(s) = sL I(s)$ $I(s) = \frac{1}{sL} V(s)$

- Inductor doesn't allowed sudden change of current, until impulse of voltage is applied.
- It stores energy in the form of magnetic field.
- Power dissipation in ideal inductor is zero.

Transformer: 4 terminal or 2-port devices.



$N_1 > N_2$: Step down transformer

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

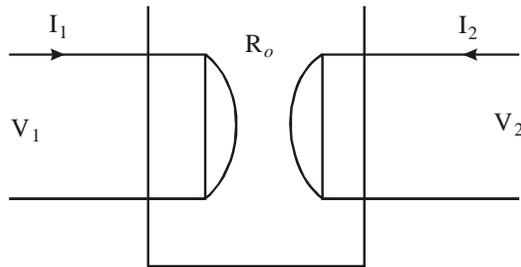
$N_2 > N_1$: Step up transformer

$$\frac{I_1}{I_2} = \frac{N_2}{N_1}$$

Where $\frac{N_1}{N_2} = K \rightarrow$ Turns ratio.

Transformer doesn't work as amplifier because current decreases in same amount power remain constant.

Gyrator:



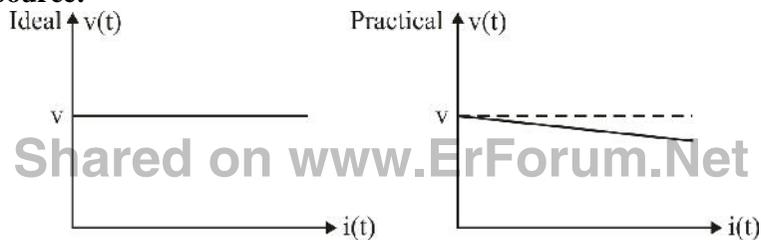
$R_o \rightarrow$ Coefficient of Gyrator

$$V_1 = R_o I_2$$

$$V_2 = -R_o I_1$$

- If load is capacitive then input impedance will be inductive and vice versa.
- If load is inductive then input impedance will be capacitive.
- It is used for simulation of equivalent value of inductance.

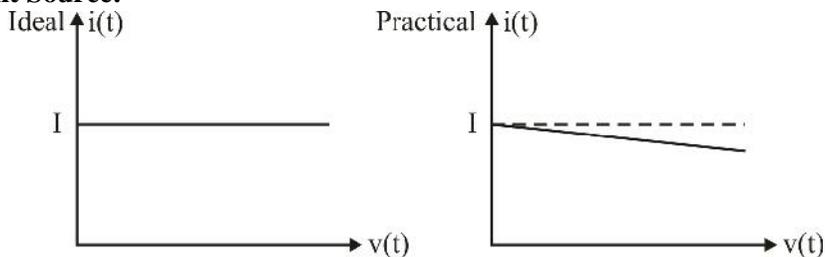
Voltage Source:



In practical voltage source, there is small internal resistance, so voltage across the element varies with respect to current.

- **Ideal voltmeter, $R_v \rightarrow \infty$ (Internal resistance)**

Current Source:



In practical current source, there is small internal resistance, so current varies with respect to the voltage across element.

- **Ideal Ammeter, $R_a \rightarrow 0$ (Internal resistance)**

Dependent and Independent Source:

Independent Source: Voltage or current source whose values doesn't depend on any other parameters. E.g. Generator etc.

Dependent Source: Voltage or current source whose values depend upon other parameters like current, voltage.

The handling of independent and dependent voltage source is identical except.

(i) In Thevenin and Norton Theorem

(ii) Superposition Theorem

Where, (i) All **independent** voltage sources are short circuited.

(ii) All **independent** current sources are open circuited.

(iii) All **dependent** voltage and current sources are left as they are.

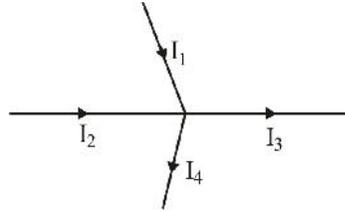
- A network in which all network elements are physically **separable** is known as **lumped network**.
- A network in which the circuit elements like resistance, inductance etc, are not physically separate for analysis purpose, is called **distributed network**. E.g. Transmission line.
- If an element is capable of delivering energy independently, then it is called active element.
Example: Voltage source, Current source
- If it is not capable of delivering energy, then it is **passive element**.
Example: Resistor, Inductor, Capacitor
- If voltage and current across an element are related to each other through a constant coefficient then the element is called as **linear element** otherwise it is called as **non-linear**.
- When elements characteristics are independent of direction of current then element is called **bi-directional** element otherwise it is called as **unidirectional**.
Ex: R, L & C.
- Diode is a unidirectional element.
- Voltage and current sources are also **unidirectional** elements.
- Every linear element should obey the **bi-directional** property but vice versa as is not necessary.
- Internal resistance of **voltage source** is in series with the source. Internal resistance of ideal **voltage source** is zero.
- Internal resistance of **current source** is in parallel with the source. Internal resistance of ideal **current source** is infinite.

2. METHODS OF ANALYSIS AND THEOREMS

(i) **Kirchoff's Points Law or Current Law (KCL):** In any electrical network, the algebraic sum of the currents meeting at point (or junction) is zero.

Incoming current = Outgoing current

$$I_1 + I_2 = I_3 + I_4$$



It is based on conservation of charge.

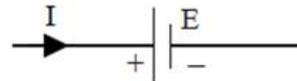
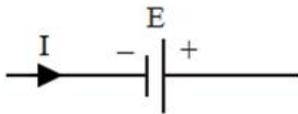
(ii) **Kirchoff's Mesh Law or Voltage Law (KVL):** The algebraic sum of products of currents and resistance in each of conductor in any closed path in a network plus the algebraic sum of emf in that path is zero.

$$\text{i.e. } \Sigma IR + \Sigma \text{emf} = 0$$

It is based on conservation of energy.

Determination of Voltage Sign

(a) **Sign of Battery E.M.F.:**



Rise in voltage

Drop in voltage

(b) **Sign of IR Drop:**



Resistors in Series:

$$R_{\text{eq}} = R_1 + R_2 + R_3 + \dots + R_n$$

Resistors in Parallel:

$$\frac{1}{R_{\text{eq}}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \dots + \frac{1}{R_n}$$

Inductors in Series:

$$L_{\text{eq}} = L_1 + L_2 + L_3 + \dots + L_n$$

Inductors in Parallel:

$$\frac{1}{L_{\text{eq}}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \dots + \frac{1}{L_n}$$

Capacitors in Series:

$$\frac{1}{C_{\text{eq}}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \dots + \frac{1}{C_n}$$

Capacitor in Parallel:

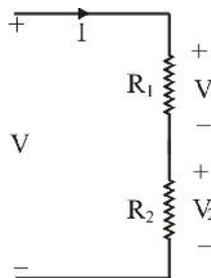
$$C_{\text{eq}} = C_1 + C_2 + C_3 + \dots + C_n$$

Voltage Divider:

$$V = V_1 + V_2$$

$$V_1 = \frac{R_1 V}{R_1 + R_2}$$

$$V_2 = \frac{R_2 V}{R_1 + R_2}$$

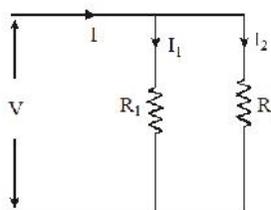


Current Divider:

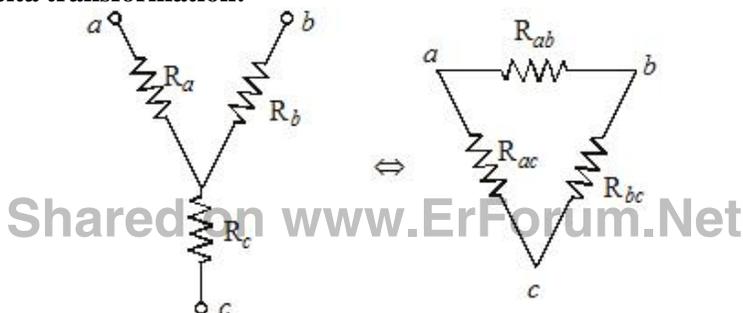
$$I = I_1 + I_2$$

$$I_1 = \frac{R_2}{R_1 + R_2} I$$

$$I_2 = \frac{R_1}{R_1 + R_2} I$$



Star to Delta transformation:



$$R_{ab} = \frac{\Delta}{R_c}, R_{bc} = \frac{\Delta}{R_a}, R_{ca} = \frac{\Delta}{R_b}$$

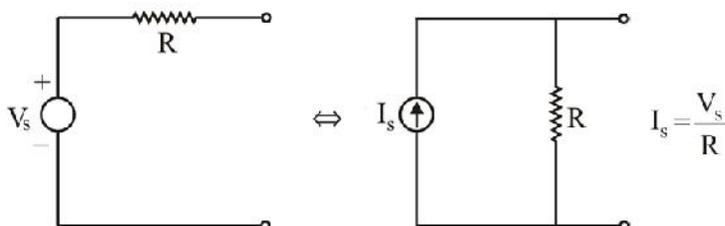
where

$$\Delta = R_a R_b + R_b R_c + R_c R_a$$

Delta to Star Transformation:

$$R_a = \frac{R_{ca} R_{ab}}{R_{ab} + R_{bc} + R_{ca}} \quad R_b = \frac{R_{ab} R_{bc}}{R_{ab} + R_{bc} + R_{ca}} \quad R_c = \frac{R_{bc} R_{ca}}{R_{ab} + R_{bc} + R_{ca}}$$

Source Transformation: Transformation of voltage source to current source or vice versa.



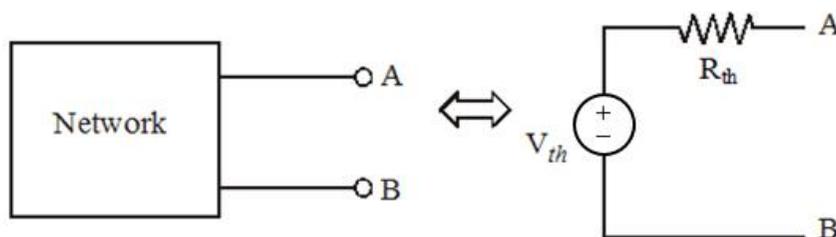
Superposition Theorem:

The response (current or voltage) in any element of a linear, bilateral R, L, C network containing more than one independent or dependent voltage or current sources is the algebraic sum of the response produced by various sources each acting alone.

- This theorem is not valid for non-linear elements, non linear parameters such as power.
- It is not valid for unilateral elements.

Thevenin's Theorem:

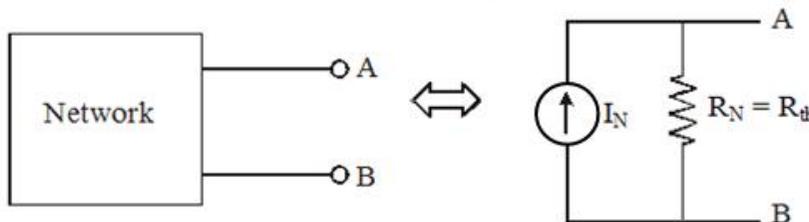
It is used to represent a linear bilateral network by an equivalent circuit having a voltage source and resistance in series with it.



V_{th} → Open circuit voltage across AB.

R_{th} → Equivalent impedance seen from terminal AB by replacing all sources by their internal impedance.

Norton's Theorem: It is used to represent a linear bilateral network by an equivalent circuit having a current source and impedance in parallel with it.



I_N → Short circuit current through terminal AB.

R_N → Equivalent impedance seen from terminal AB by replacing all their sources by their internal impedance.

- For finding R_N or R_{th} when there are dependent voltage or current source:

Keep the dependent voltage or current source as it is and short or open appropriate independent sources and applied a D.C. 1V voltage source or 1A current source at open circuit terminals, where R_N or R_{th} is to be determined i.e. at AB terminals.

$$R_N \text{ or } R_{th} = \frac{V_{d.c.}}{I_{d.c.}}$$

- With no independent sources in the Thevenin's and Norton's model the Thevenin's voltage become $V_{th} = 0$ and we can only find R_{th} in these types of circuits.

2

CONTROL SYSTEMS

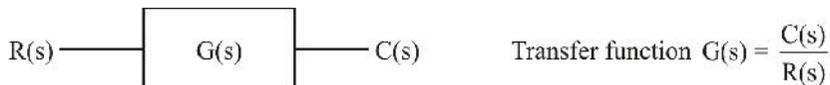
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1. BLOCK DIAGRAM

Open Loop Control System:

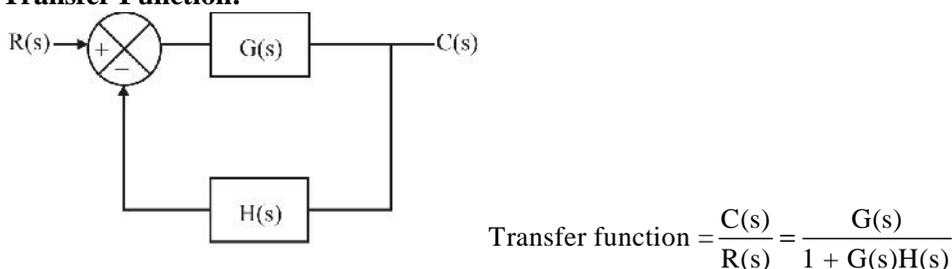
- In this system the output is not feedback for comparison with the input.
- Open loop system faithfulness depends upon the accuracy of input calibration.



When a designer designs, he simply design open loop system.

Closed Loop Control System: It is also termed as feedback control system. Here the output has an effect on control action through a feedback. Ex. Human being

Transfer Function:



Comparison of Open Loop and Closed Loop control systems:

Open Loop:

1. Accuracy of an open loop system is defined by the calibration of input.
2. Open loop system is simple to construct and cheap.
3. Open loop systems are generally stable.
4. Operation of this system is affected due to presence of non-linearity in its elements.

Closed Loop:

1. As the error between the reference input and the output is continuously measured through feedback. The closed system works more accurately.
2. Closed loop systems is complicated to construct and it is costly.
3. It becomes unstable under certain conditions.
4. In terms of performance the closed loop system adjusts to the effects of non-linearity present.

Transfer Function: The transfer function of an LTI system may be defined as the ratio of Laplace transform of output to Laplace transform of input under the assumption

$$G(s) = \frac{Y(s)}{X(s)}$$

- The transfer function is completely specified in terms of its poles and zeros and the gain factor.

- The T.F. function of a system depends on its elements, assuming initial conditions as zero and is independent of the input function.
- To find a gain of system through transfer function put $s = 0$

Example: $G(s) = \frac{s + 4}{s^2 + 6s + 9}$ Gain = $\frac{4}{9}$

If a step, ramp or parabolic response of T.F. is given, then we can find Impulse Response directly through differentiation of that T.F.

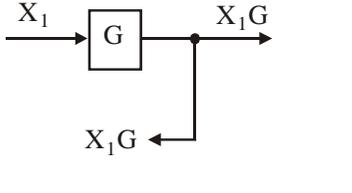
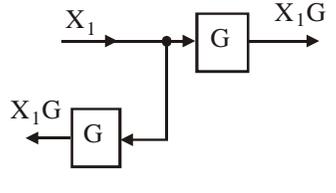
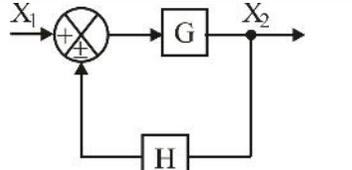
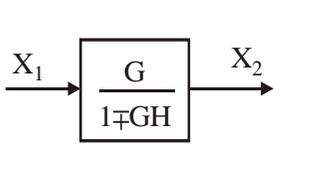
$$\frac{d}{dt} \text{ (Parabolic Response) = Ramp Response}$$

$$\frac{d}{dt} \text{ (Ramp Response) = Step Response}$$

$$\frac{d}{dt} \text{ (Step Response) = Impulse Response}$$

Block Diagram Reduction:

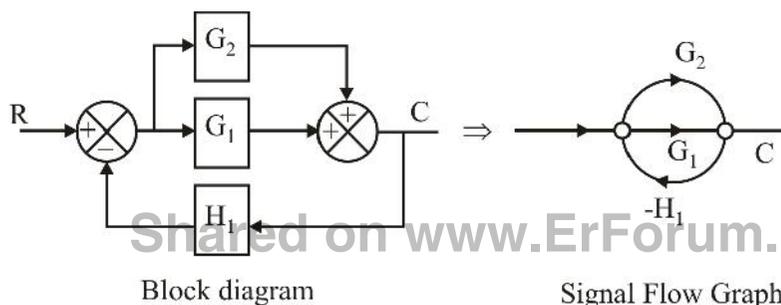
Rule	Original Diagram	Equivalent Diagram
1. Combining blocks in cascade		
2. Moving a summing point after a block		
3. Moving a summing point ahead of block		
4. Moving a take off point after a block		

<p>5. Moving a take off point ahead of a block</p>		
<p>6. Eliminating a feedback loop</p>		

$(GX_1 \pm X_2)$

Signal Flow Graphs:

- It is a graphical representation of control system.
- Signal Flow Graph of Block Diagram:



Mason's Gain Formula: Transfer function = $\frac{\sum p_k \Delta_k}{\Delta}$

$p_k \rightarrow$ Path gain of k^{th} forward path

$\Delta = 1 - [\text{Sum of all individual loops}] + [\text{Sum of gain products of two non-touching loops}] - [\text{Sum of gain products of 3 non-touching loops}] + \dots$

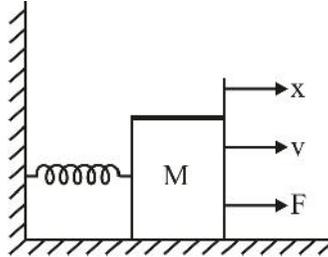
$\Delta_k \rightarrow$ Value of Δ obtained by removing all the loops touching k^{th} forward path as well as non-touching to each other

2. MATHEMATICAL MODELLING

Mechanical System:

Translational System:

Mass:



$$F = m \frac{d^2x}{dt^2} = m \frac{dv}{dt}$$

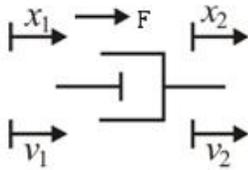
F = Force on block m

V = Velocity of Block

x = Displacement of block

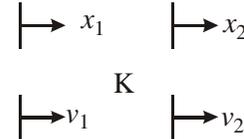
m = Mass of block

Damper



$$F = f \frac{d}{dt}(x_1 - x_2)$$

Spring



by hooke's law

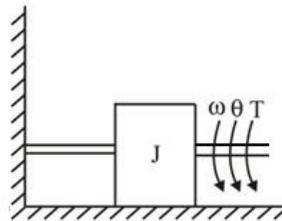
$$F = k(x_1 - x_2) = k \int (v_1 - v_2) dt$$

k → Spring constant

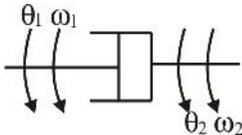
Rotational System

Inertia

$$T = J \frac{d^2\theta}{dt^2} = J \frac{d\omega}{dt}$$

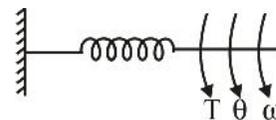


Damper



$$T = f \frac{d^2\theta}{dt^2} = f(\omega_1 - \omega_2)$$

Spring twisted:



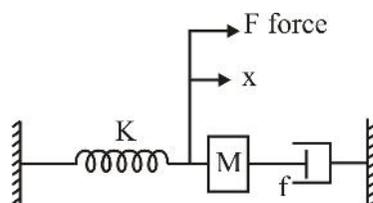
$$T = k\theta = k \int \omega dt$$

Force Voltage and Force Current Analogy:

Voltage (Series RLC)	Current (Parallel RLC)	Force (Translational)	Torque (Rotational)
V	I	F	T
q	ϕ	x	θ
R	$\frac{1}{R}$	f (Damper)	f (Damper)
$\frac{1}{C}$	$\frac{1}{L}$	k	k
L	C	M	J
I	V	Linear velocity	Angular velocity

Conversion of Translational System to other Systems:

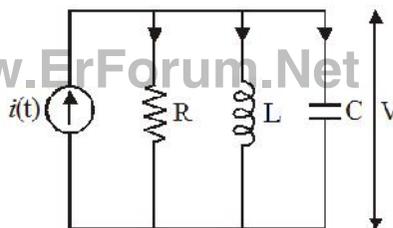
$$F = M \frac{d^2x}{dt^2} + f \frac{dx}{dt} + kx$$



Force–Current Analogy:

$$i = C \frac{d^2w}{dt^2} + \frac{1}{R} \frac{dw}{dt} + \frac{w}{L}$$

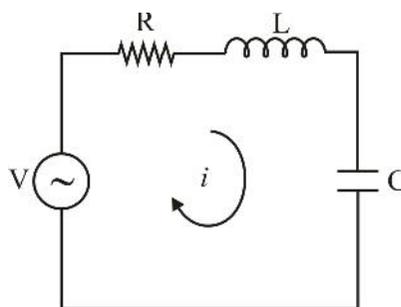
$$i = C \frac{dv}{dt} + \frac{v}{R} + \frac{1}{L} \int v dt$$



Force–Voltage Analogy:

$$V = L \frac{d^2q}{dt^2} + R \frac{dq}{dt} + \frac{q}{C}$$

$$V = L \frac{di}{dt} + iR + \frac{1}{C} \int i dt$$

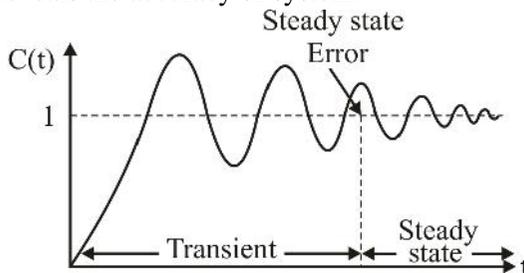


3. TIME RESPONSE ANALYSIS

- Time Response is divided in two parts.

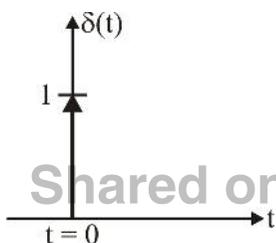
1. Transient Response: It reveals the nature of response (oscillating or overdamped) and also gives indication about its speed.

2. Steady State: It reveals the accuracy of system.



Standard Input Test Signals:

1. Impulse signal:

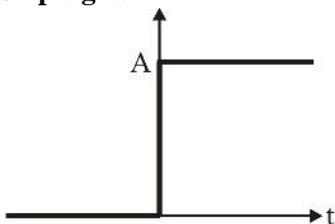


$$u(t) = \begin{cases} 1, & t = 0 \\ 0, & t \neq 0 \end{cases}$$

$$\int_{-\infty}^{+\infty} u(t) dt = 1$$

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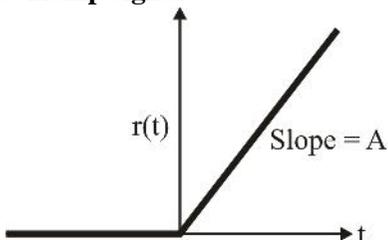
2. Step signal:



$$R(t) = A u(t)$$

Also called displacement function

3. Ramp signal:



$$R(t) = A t u(t)$$

Also called velocity function

3

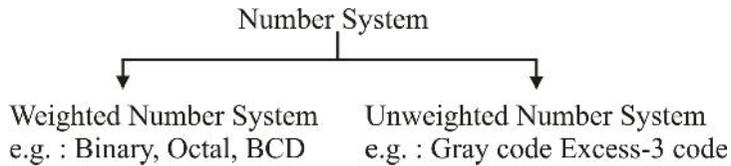
DIGITAL ELECTRONICS AND CIRCUITS

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1. NUMBER SYSTEM & CODES

Number System and Codes:



A number system with base ' r ', contains ' r ' different digits and they are from 0 to $r - 1$.

Decimal to other codes conversions: To convert decimal number into other system with base ' r ', divide integer part by r and multiply fractional part with r .

Other codes to Decimal Conversions: $(x_2x_1x_0 \cdot y_1y_2)_r \rightarrow (A)_{10}$

$$A = x_2r^2 + x_1r + x_0 + y_1r^{-1} + y_2r^{-2}$$

Hexadecimal to Binary: Convert each Hexadecimal digit into 4 bit binary.

$$(5AF)_{16} \rightarrow \frac{(0101)}{5} \frac{(1010)}{A} \frac{(1111)}{F}_2$$

Binary to Hexadecimal: Grouping of 4 bits into one hex digit.

$$(11010111)_2 \rightarrow \underbrace{0011}_{3} \underbrace{0101}_{5} \underbrace{1100}_{C} \rightarrow (35.C)_{16}$$

Octal to Binary and Binary to Octal: Same procedure as discussed above but here group of 3 bits is made.

Codes:

Binary coded decimal (BCD):

- In BCD code each decimal digit is represented with 4 bit binary format.

$$Eg : (943)_{10} \rightarrow \left(\underbrace{1001}_9 \underbrace{0100}_4 \underbrace{0011}_9 \right)_{BCD}$$

- It is also known as 8421 code

Invalid BCD codes

Total Number possible $\rightarrow 2^4 \Rightarrow 16$

Valid BCD codes $\rightarrow 10$

Invalid BCD codes $16 - 10 \Rightarrow 6$

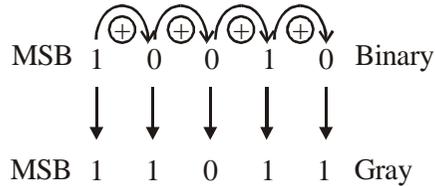
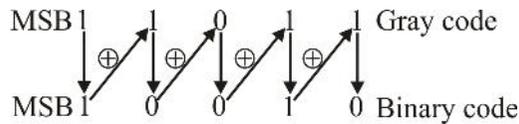
These are 1010, 1011, 1100, 1101, 1110, and 1111

Excess-3 code: (BCD + 0011)

- It can be derived from BCD by adding '3' to each coded number.
- It is unweighted and self-complementing code.

Gray Code:

It is also called minimum change code or unit distance code or reflected code.

Binary code to Gray code:**Gray code to Binary code:****Alpha Numeric codes: EBCDIC (Extended BCD Interchange code)**

It is 8 bit code. It can represent 128 possible characters.

- Parity Method is most widely used schemes for error detection.
- Hamming code is most useful error correcting code.
- BCD code is used in calculators, counters.

Complements: If base is r then we can have two complements.

- $(r - 1)$'s complement.
- r 's complement.

To determine $(r-1)$'s complement: First write maximum possible number in the given system and subtract the given number.

To determine r 's complement: $(r-1)$'s complement + 1

First write $(r-1)$'s complement and then add 1 to LSB

Example: Find 7's and 8's complement of 2456

$$\begin{array}{r} 7777 \\ -2456 \\ \hline 5321 \end{array} \qquad \begin{array}{r} 5321 \\ +1 \\ \hline 5322 \end{array}$$

Find 2's complement of 101.110

1's complement 010.001

For 2's complement add 1 to the LSB

$$\begin{array}{r} 010.001 \\ +1 \\ \hline 010.010 \end{array}$$

2. BINARY AIRTHMETIC

When both the numbers have same sign then we add only magnitude and use the sign of MSB.

1' Complement Addition: When the numbers have different signs, keep one number as it is and take 1's complement of the negative number and add them.

If carry occurs:

(a) add carry to LSB

(b) sign of the result is sign of the complemented number.

If carry does not occur:

(a) take 1's complement of the result

(b) sign of the result is sign of the complemented number.

2' Complement Addition: When the numbers have different signs, keep the positive number as it is and take 2's complement of the negative number and add them.

If carry occurs:

(a) carry is discarded

If carry does not occur:

(a) take 2's complement of the result

(b) sign of the result is sign of the complemented number

BCD Addition: Add the BCD numbers as regular true binary numbers.

If the sum is 9(1001) or less, it is a valid BCD answer.

If sum is greater than 9 or if there is carryout of MSB, it is an invalid BCD number.

If it is invalid, add 6 (0110) to the result to make it valid. Any carry out of the MSB is added to the next more-significant BCD number.

Repeat steps for each group of BCD bits

$$\begin{array}{r}
 76 \quad 0111 \ 0110 \\
 +94 \quad + 1001 \ 0100 \\
 \hline
 170 \quad 1 \ 0000 \ 1010
 \end{array}$$

Invalid BCD number

Add 6 (110) in the result,

$$\begin{array}{r}
 1 \ 0000 \ 1010 \\
 + 0110 \ 0110 \\
 \hline
 1 \ \underbrace{0111}_7 \ \underbrace{0000}_0
 \end{array}$$

valid BCD number

Overflow concept: Overflow may occur when two same sign numbers are added.

Overflow condition : If x and y are the MSB's of two numbers and z is resultant MSB after adding two numbers then overflow conditions is

$$\bar{x} \bar{y} z + x y \bar{z} = 1$$

BOOLEAN ALGEBRA

Basic Operations:

AND	OR	NOT
$A.A=A$	$A+A=A$	
$A.0=0$	$A+0=A$	$\overline{\overline{A}}=A$
$A.1=A$	$A+1=1$	
$A.\bar{A}=0$	$A+\bar{A}=1$	

Boolean algebra Laws:

Commutative Law: $A + B = B + A$ and $A.B = B.A$

Associative Law: $A + (B + C) = (A + B) + C = A + B + C$
 $A.(B.C) = (A.B).C = A.B.C$

Distributive Law: $A.(B + C) = A.B + A.C$

Theorems: Distribution theorem: $(A + B).C = (A + B).C$
 $A.(B + C) = A.B + A.C$

Example: $(\bar{A} + \bar{A}B) = (\bar{A} + A)(\bar{A} + B) = (\bar{A} + B)$

$$A + \bar{A}B = (A + \bar{A})(A + B) = A + B$$

Transposition Theorem: $(A + B) . (A + C) = A + B.C$

De Morgan's Law:

$$\overline{A_1.A_2.A_3.....A_n} = \bar{A}_1 + \bar{A}_2 + \dots + \bar{A}_n$$

$$\overline{A_1 + A_2 + A_3..... + A_n} = \bar{A}_1 . \bar{A}_2 . \dots . \bar{A}_n$$

Involution Theorem: $\overline{\bar{A}} = A$

Absorption Theorem: $A + AB = A$

Dual Expression: It will convert positive logic into negative and negative logic into positive logic.

Procedure:

1. Change each OR sign by AND and vice-versa.
2. Convert all 1s to 0s and all 0s to 1s.
3. Keep variables as it is.

- If one time dual is as same as function then it is known as **self dual expression**.

Boolean Function Representation:

Canonical Form: All terms contain each literal.

$$F(A, B, C) = \bar{A}BC + A\bar{B}C + A\bar{B}\bar{C}$$

Standard form: All the terms do not have each literal.

$$F(A, B, C) = \bar{A} + BC + A\bar{B}C$$

Sum of Product (SOP) :

- In SOP form each product term is known as minterm.
- SOP forms are used to write logical expression so that the output becomes logic '1'.
- Notation for SOP expression is $f(A, B, C) = \sum m(3, 5, 6, 7)$

$$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

Product of Sum (POS):

Example: $(A + \bar{C}) \cdot (\bar{B} + E)$

- Each individual term in standard POS is called maxterm.
- POS forms are used to write logical expression so that the output becomes logic '0'.

Example: $f(A, B, C) = \pi M(0, 1, 2, 4)$

$$Y = (A + B + C) (A + B + \bar{C}) (A + \bar{B} + C) (\bar{A} + B + C)$$

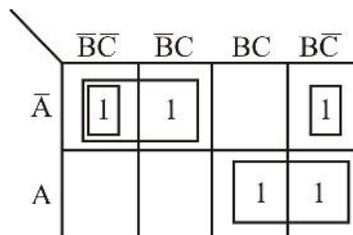
Implicant: Each individual minterm or group of minterms in canonical SOP is called implicant.

Prime Implicant: It is a minterm, which are obtained by combining maximum possible adjacent cells in *k*-map.

Essential Prime Implicant: It is Prime Implicant in which one or more minterms are unique.

Example:

1.



Possible K-map solutions:

$$AB + \bar{A}\bar{B} + B\bar{C}$$

$$AB + \bar{A}\bar{B} + \bar{A}\bar{C}$$

PI: $\bar{A}\bar{B}, \bar{A}\bar{C}, AB, B\bar{C}$

EPI: $\bar{A}\bar{B}, AB$

2.

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	1		
A	1	1	1	1

PI: A, \bar{B} **EPI:** A, \bar{B}

- **With n Variable**

Maximum possible logic expressions $\rightarrow 2^{2^n}$ Minterms/Maxterms $\rightarrow 2^n$ Self dual expressions $\rightarrow 2^{2^n-1}$

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ANALOG ELECTRONICS

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1. VOLTAGE REGULATOR & RECTIFIERS

Voltage Regulator Circuits:

$$\% \text{ Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

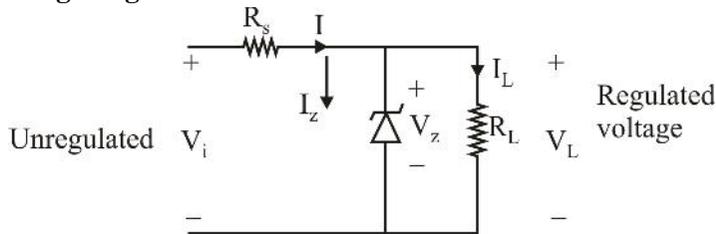
$$\text{Full load current} = I_{FL} = \frac{V_{FL}}{R_L}$$

V_{NL} -No load

V_{FL} -Full load

Smaller the regulation better is the circuit performance.

Zener Voltage Regulator Circuit:



Since Zener diode is conducting

$$V_L = V_z = V_{Br}$$

$$V_L = I_L R_L$$

$$V_z = I_z R_z$$

$$I = I_z + I_L$$

If Zener current is maximum then load current is minimum and vice versa.

$$I = I_{z \max} + I_{L \min}$$

$$I = I_{z \min} + I_{L \max}$$

For satisfactory operation of circuit

$$I \geq I_{z \min} + I_L$$

$$\frac{V_i - V_L}{R_s} \geq I_{z \min} + I_L$$

The power dissipated by the Zener diode is

$$P_z = V_z I_z$$

Rectifier: To convert a bi-directional current or voltage into a unidirectional current or voltage

Ripple factor:

$$r = \frac{\text{rms value of AC component}}{\text{DC value}}$$

$$r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

Form factor:

$$F = \frac{\text{rms value}}{\text{dc value}} = \frac{V_{rms}}{V_{dc}} \quad r = \sqrt{F^2 - 1}$$

$$\text{Crest factor} = \frac{\text{Peak value}}{\text{RMS value}}$$

$$\text{Rectifier Efficiency} = \frac{\text{DC power output}}{\text{AC power input}} \times 100\%$$

TUF (Transformer utilization factor):

$$\text{TUF} = \frac{\text{DC power output}}{\text{AC rating of transformer}}$$

Half Wave Rectifier: Average value of current and voltage

$$I_{\text{dc}} = \frac{I_m}{\pi}, \quad V_{\text{dc}} = \frac{V_m}{\pi}$$

RMS value of current and voltage: $I_{\text{rms}} = \frac{I_m}{2}, \quad V_{\text{rms}} = \frac{V_m}{2}$

Efficiency $\eta = 40.6\%$

Ripper factor = 1.21

Frequency of ripple voltage = f

Form factor = 1.57

Peak inverse voltage = V_m

TUF = 0.286

Full Wave Rectifier: Average value of current and voltage:

$$I_{\text{dc}} = \frac{2I_m}{\pi}, \quad V_{\text{dc}} = \frac{2V_m}{\pi}$$

RMS value of current and voltage: $V_{\text{rms}} = \frac{V_m}{\sqrt{2}}, \quad I_{\text{rms}} = \frac{I_m}{\sqrt{2}}$

Efficiency $\eta = 81.2\%$

Ripper factor = 0.48

From factor = 1.11

Crest factor = $\sqrt{2}$

TUF = 0.692

Frequency of ripple voltage = $2f$

Peak inverse voltage = $2V_m$

Bridge Rectifier: All the parameters are same as full wave rectifier except

Peak inverse voltage = V_m Transformer utilization factor = 0.812

Advantage of Bridge Rectifier:

1. The current in both the primary and secondary of the transformer flows for entire cycle.
2. No center tapping is required in the transformer secondary. Hence it is a cheap device.
3. The current in the secondary winding of transformer is in opposite direction in two half cycles. Hence net DC current flow is zero.
4. As two diode currents are in series, in each of the cycle inverse voltage appear across diode gets shared. Hence the circuit can be used for high voltage application.

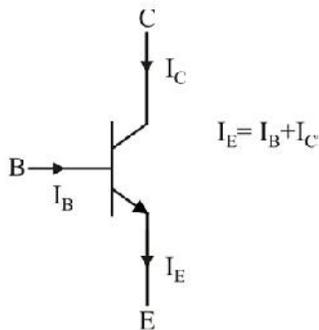
2. BJT & TRANSISTOR BIASING

General Equation of Transistor: **In CE mode** → $I_C = I_B + (1 + \beta) I_{CO}$

In CB mode → $I_C = \alpha I_E + I_{CO}$

$$I_E = I_{CO} e^{\frac{V_{BE}}{V_T}}$$

Typical values for $V_{BE} =$ 0.2 (Ge Transistor)
 0.7 (Si Transistor)
 1.3 (GaAs Transistor)



(a) Condition to keep transistor in **cut off**: $V_{BE} < 0.7V$

(b) Condition for transistor under **active region**:

1. $V_{BE} = 0.7V$
2. $I_C = \beta I_B = \alpha I_E$
3. $I_B < \frac{I_{C\text{sat}}}{\beta}$

(c) Transistor under **saturation region**:

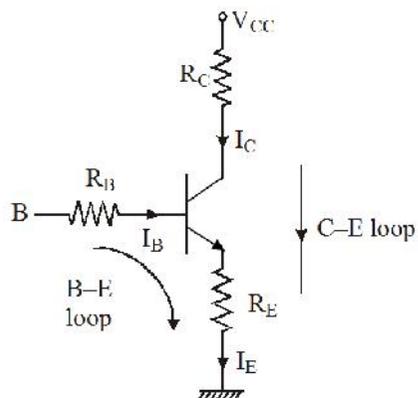
To find whether transistor is in active mode or saturation mode

$$V_{BE} = 0.7V$$

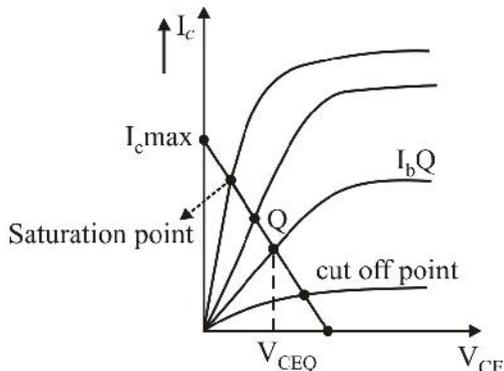
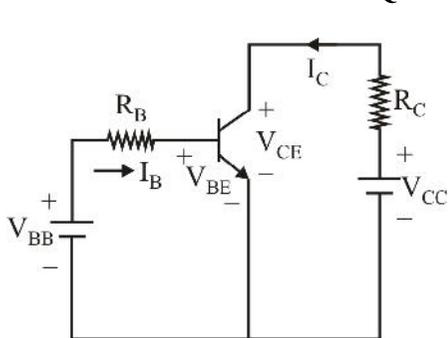
$$I_C \neq \beta I_B \neq \alpha I_E$$

$$V_{CE\text{sat}} = 0.2V$$

- I. If $I_C \text{ active} > I_C \text{ (saturation)}$
 then transistor is in saturation and Q point is $(I_C \text{ (saturation)}, 0.2)$.
- II. If $I_C \text{ (saturation)} > I_C \text{ (active)}$
 then transistor is in active region and Q point is $(I_C \text{ (active)}, V_{CE})$.



Transistor DC Load Line and Q Point



- DC load line is a straight line which joins I_{cmax} and V_{CC} or which joins saturation and cutoff point.
- DC load line is the locus of all possible operating point at which it remains in active region.
- Q point is called quiescent point or operating point and it is a function of I_B , I_C , and V_{CC} .
- For best performance of amplifier in the BJT the Q point must be located at the center of D.C. load line.

Stability Factor:

I_C is a function of I_{CO}, V_{BE}, S (Temperature dependent parameter)

$$\text{Stability } S = \left. \frac{\partial I_C}{\partial I_{CO}} \right|_{V_{BE}, S}$$

Smaller the values of S better will be thermal stability.

The general equation for **stability factor S**:

$$S = \frac{1 + S}{1 - S \frac{\partial I_B}{\partial I_C}}$$

Transistor Biasing Circuits and Their Stability:

A. Fixed Bias Circuit (Base – Bias)

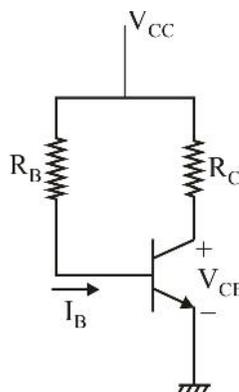
$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Stability

$$S = 1 + S$$

Fixed bias circuit is unstable.



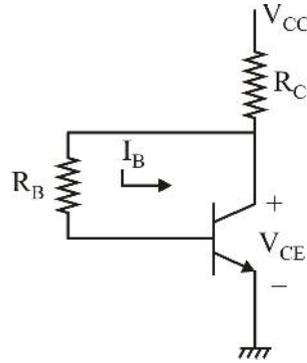
B. Collector to base bias circuits

$$I_B = \frac{V_{CC} - V_{BE}}{(S + 1)R_C + R_B}$$

$$I_C \approx SI_B$$

Stability

$$S = \frac{1 + S}{1 + S \frac{R_C}{R_C + R_B}}$$



The circuit is having good thermal stability.

C. Self bias circuit → (Potential divider bias circuit)

Emitter bias circuit

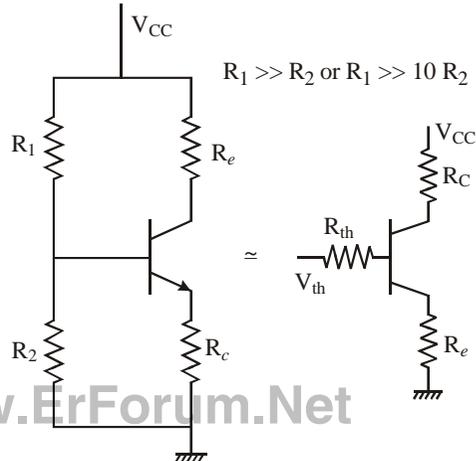
It is popularly used in biasing circuit.

It gives 180° phase shift.

when,

$$V_{th} = \frac{V_{CC}R_2}{R_1 + R_2} \quad R_{th} = \frac{R_1R_2}{R_1 + R_2}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E} \quad I_E = \frac{V_{th} - V_{BE}}{R_E + \left(\frac{R_{th}}{B + 1}\right)}$$



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Stability factor

$$S = \frac{1 + S}{1 + S \frac{R_E}{R_{th} + R_E}} = \frac{S}{S \frac{R_E}{R_E + R_{th}}}$$

$$S = 1 + \frac{R_{th}}{R_E}$$

Thermal Runway:

- The self destruction of the transistor due to the excess heat produced within the device is called thermal runaway.
- It is due to I_{CO}
- BJT suffers from thermal runaway.
- In FET, there is no thermal runaway.

Conditions to eliminate thermal runaway: $V_{CE} \leq \frac{V_{CC}}{2}$ & $\frac{\partial P_C}{\partial T_j} < \frac{1}{\dots}$

Thermal resistance (θ)

$$\theta = \frac{T_j - T_A}{P_D} \left(\text{ }^\circ\text{C} / \text{watt or } \text{K} / \text{watt} \right)$$

$T_j \rightarrow$ Junction temperature (collector junction)

$T_A \rightarrow$ Ambient temperature

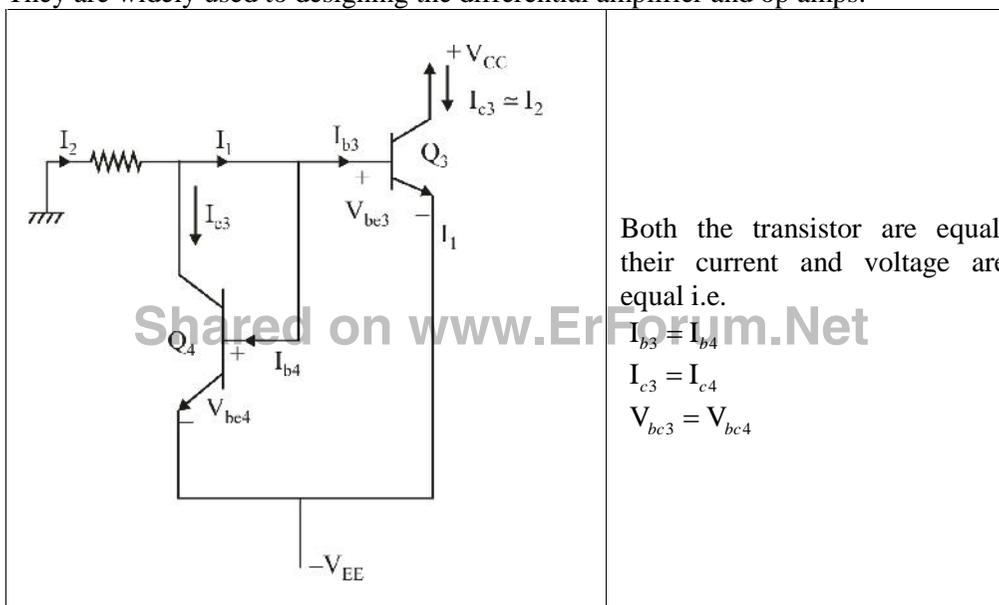
$P_D \rightarrow$ Power dissipated across collector junction

A transistor is thermally stable if $\frac{dP_C}{dT_j} \leq \frac{dP_D}{dT_j}$

$\frac{dP_C}{dT_j} \rightarrow$ Rate at which heat is released $\frac{dP_D}{dT_j} \rightarrow$ Rate at which heat is dissipated

Current Mirror Circuit: In current mirror circuit, the output current is forced to approximately equal to the input current.

They are widely used to designing the differential amplifier and op amps.



Both the transistor are equal, their current and voltage are equal i.e.

$$I_{b3} = I_{b4}$$

$$I_{c3} = I_{c4}$$

$$V_{be3} = V_{be4}$$

$$I_2 = I_{c4} + I_1$$

$$I_2 = I_{c4} + 2I_{b4}$$

$$I_2 = I_{c3} + 2I_{b3}$$

$$I_2 = I_{c3} \left(1 + \frac{2}{\beta} \right)$$

$$I_{c3} = \frac{I_2}{1 + \frac{2}{\beta}}$$

$$I_1 = I_{b3} + I_{b4}$$

$$I_{c3} = I_{c4}$$

$$I_{b3} = I_{b4}$$

If β is large

$$I_{c3} \approx I_2$$

11

ELECTICAL MACHINES

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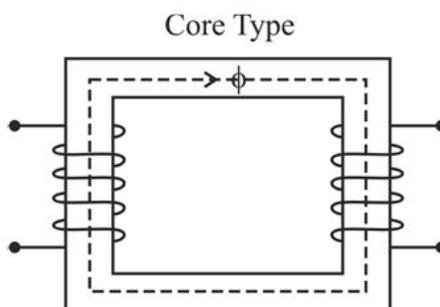
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1. TRANSFORMER

Definition: A transformer is a static device that transfers electrical energy from one electrical circuit to another electrical circuit through the medium of magnetic field and without the change of frequency.

Construction of Transformer:

Core Type:

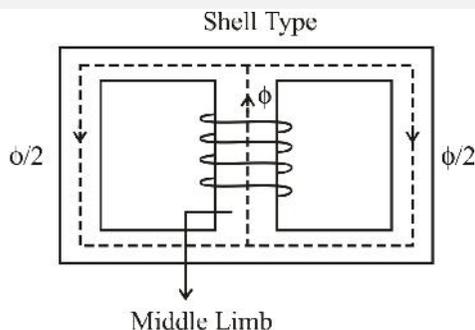


1. In core type construction, both the limbs are provided with windings and the core is surrounded by windings.
2. For a given output and voltage rating, it requires less iron but more copper.
3. Cross-section area of both limbs is equal.
4. These are used for high power applications.
5. These are suited for high voltage, small kVA rating.

For example: 15 kVA, 2200 / 1100 V

6. Cost of insulation is less.

Shell Type:



1. In shell type, only middle limb is provided with winding and the windings are surrounded by core.
2. Amount of copper required is less.
3. Cross-sectional area of the middle limb is twice to that of outer limbs.
4. These are used for low power applications.
5. These are suited for large kVA ratings but low voltage.

For Example: 150 kVA, 400/230 V

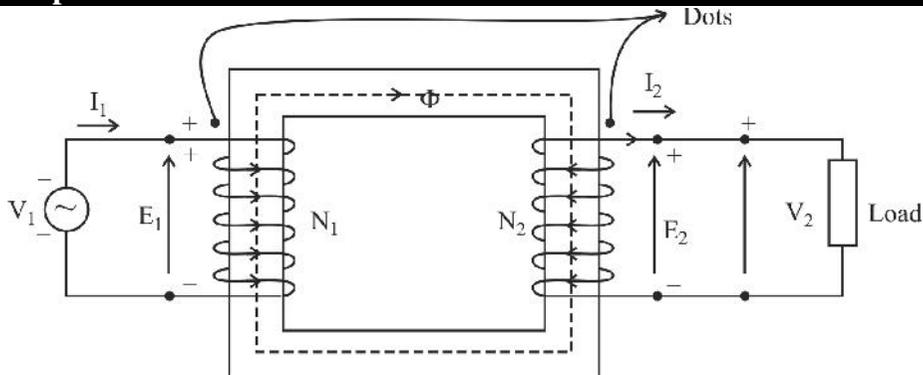
Principle of Transformer Action:

Figure (i)

- A transformer works on the principle of electromagnetic induction between two (or more) coupled circuits or coils. According to Faraday's law of electromagnetic induction, an emf is induced in a coil if it links to changing flux.
- The direction of induced emf is given by Lenz's law which states that emf will be induced in such a way that it opposes the cause which has produced it.
- In transformer electrical energy is transferred due to mutual induction between primary and secondary winding.

Emf equation of Transformer:

Referring to figure (i), E_1 = emf induced in the primary winding

E_2 = emf induced in the secondary winding

and N_1, N_2 are the winding turns.

Let the flux ϕ is represented as, $\phi = \phi_m \sin \omega t$

By Faraday's law of electromagnetic induction,

Emf induced in primary winding, $E_1 = N_1 \frac{d\phi}{dt}$

$$\Rightarrow E_1 = N_1 \frac{d}{dt} (\phi_m \sin \omega t) \quad E_1 = N_1 \omega \phi_m \cos \omega t$$

$$E_1 = (E_1)_m \sin(\omega t + 90^\circ)$$

rms value of emf induced in primary winding

$$(E_1)_{\text{rms}} = \frac{(E_1)_m}{\sqrt{2}}$$

$$(E_1)_{\text{rms}} = \sqrt{2} \pi f N_1 \phi_m \quad \dots(i)$$

Similarly, emf induced in secondary winding $E_2 = N_2 \frac{d\phi}{dt}$

$$E_2 = N_2 \omega \phi_m \sin(\omega t + 90^\circ)$$

$$(E_2)_{\text{rms}} = \left(\frac{N_2 \omega \phi_m}{\sqrt{2}} \right)$$

$$(E_2)_{\text{rms}} = \sqrt{2} \pi f N_2 \phi_m \quad \dots(ii)$$

From equation (i) and (ii), $\frac{E_1}{N_1} = \frac{E_2}{N_2}$

i.e., voltage per turns are equal in primary and secondary windings.

From figure (i) we have, $E_1 = V_1$ and $E_2 = V_2$

Hence,
$$\frac{V_1}{V_2} = \frac{E_1}{E_2} = \frac{N_1}{N_2} = a = \frac{I_2}{I_1}$$

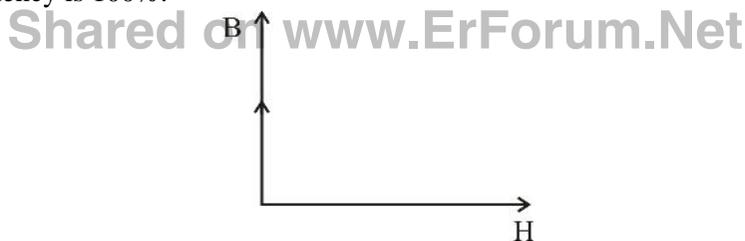
Key Points:

1. Emf induced in the windings are $\left(\frac{\pi}{2}\right)$ radians ahead by the core flux.
2. Any change in the secondary current of the transformer causes a change in primary current so that the flux remains constant.
3. Infinite permeability of the core signifies that no magnetizing current is required for establishment of flux.

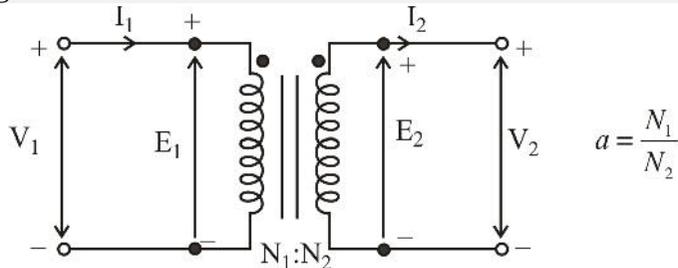
Ideal Transformer:

Properties

- (i) Resistance of the windings of transformer is zero.
- (ii) Magnetic leakage flux is zero.
- (iii) The permeability of the core of transformer is infinite.
- (iv) Efficiency is 100%.



Phasor diagram of an ideal transformer:



mmf balance equation: $N_1 \vec{I}_1 - N_2 \vec{I}_2 = 0$

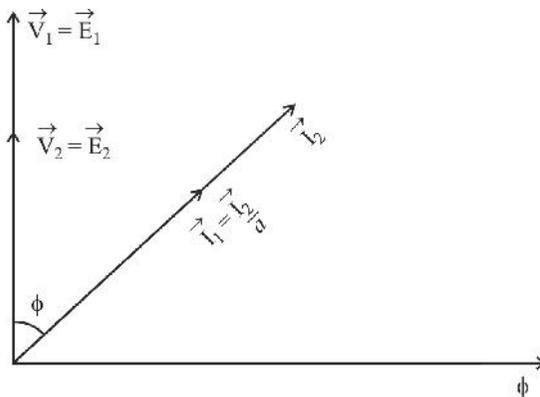
$$\Rightarrow \vec{I}_1 = \left(\frac{N_2}{N_1}\right) \vec{I}_2 = \frac{\vec{I}_2}{a} = \vec{I}_2'$$

\vec{I}_2' = Secondary current referred to primary.

Phasor diagram of a Ideal Transformer (At Lagging pf load):

Note: As per IEEE, the turns ratio (a) = $\frac{N_{HV}}{N_{LV}}$

Where, N_{HV} = Number of turns of HV winding
 N_{LV} = Number of turns of LV winding



Practical Transformer (~ 0 ζ)

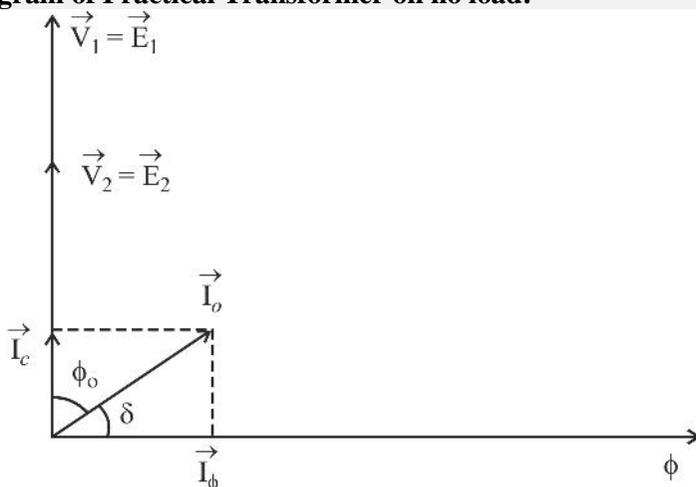
In case of a practical transformer, I_o current is required to produce flux in the core and to compensate the core losses.

The mmf balance equation reads: $N_1 \vec{I}_1 - N_2 \vec{I}_2 = N_1 \vec{I}_o$

$\Rightarrow \vec{I}_1 = \left(\frac{N_2}{N_1}\right) \vec{I}_2 + \vec{I}_o$ $\vec{I}_1 = \vec{I}_2 + \vec{I}_o$

Where I_o is the exciting current/no load current.

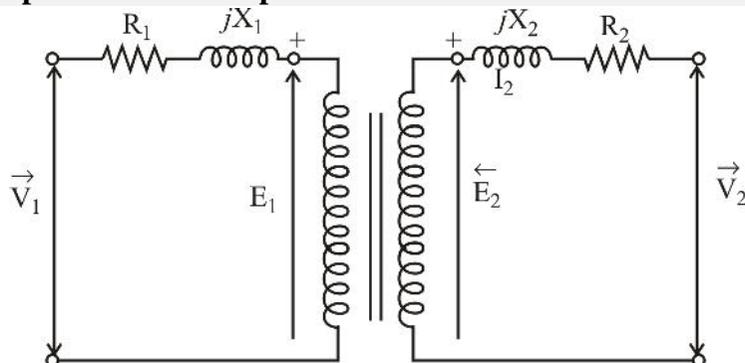
Phasor Diagram of Practical Transformer on no load:



Here, \vec{I}_c = core loss component of \vec{I}_o
 \vec{I}_ϕ = magnetizing component of \vec{I}_o

Note: Hysteresis angle (δ) shows us the lagging nature of ϕ w.r.t. I_o

Circuit Representation of a practical Transformer



The KVL equations Read:

$$\vec{E}_2 = \vec{V}_2 + I_2 R_2 + j I_2 X_2 \qquad \vec{V}_1 = \vec{E}_1 + I_1 R_1 + j I_1 X_1$$

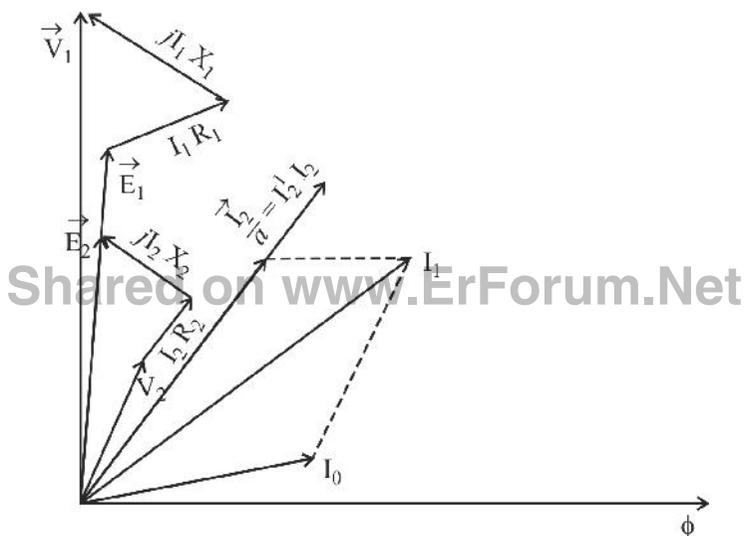


Figure: Transformer at Lagging Power Factor Load.

Equivalent circuit of Transformer:

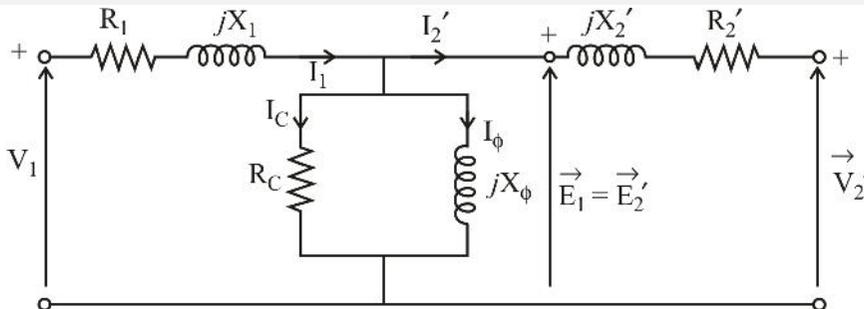


Figure: Exact equivalent circuit referred to primary side.

Here, R_2' represented the resistance of secondary winding referred to primary

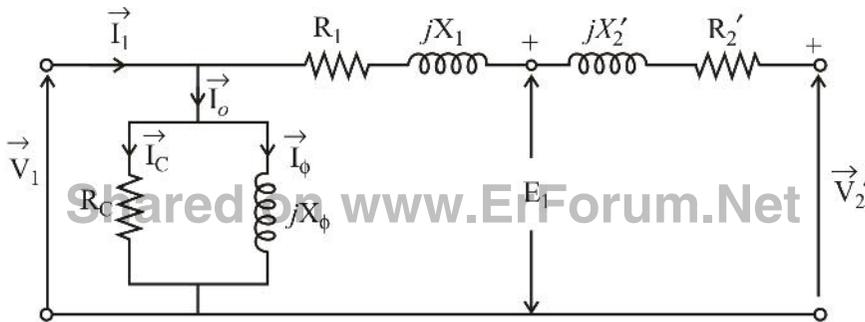
Similarly, X_2' and \vec{V}_2' represents reactance and voltage of secondary referred to primary.

Let the no. of turns on primary be N_1 and secondary be N_2

$$\begin{aligned} \text{Hence, } R_2' &= R_2 \left(\frac{N_1}{N_2} \right)^2 & X_2' &= X_2 \left(\frac{N_1}{N_2} \right)^2 \\ V_2' &= V_2 \left(\frac{N_1}{N_2} \right) & I_2' &= I_2 \left(\frac{N_2}{N_1} \right) \end{aligned}$$

Note:

- No load current (I_o) = 2% to 3% of full load current. This property of \vec{I}_o leads to further approximate circuits which are:
- The voltage drop due to I_o in (R_1+jX_1) is so small that it can be neglected.

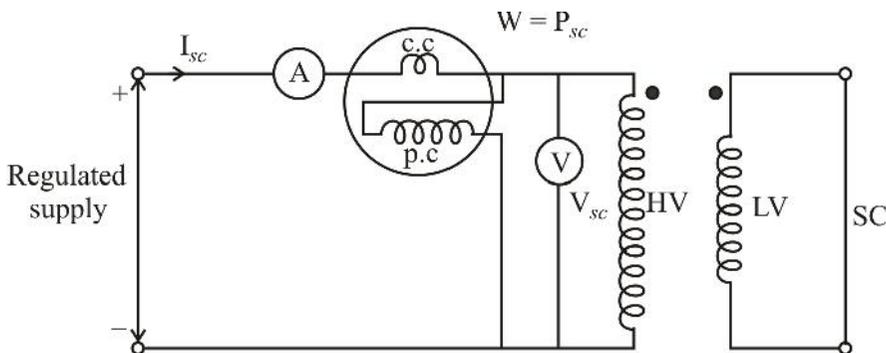


Cantilever 1st approximate circuit

Note: Due to low value of \vec{I}_o the magnetizing branch is sometimes totally ignored.

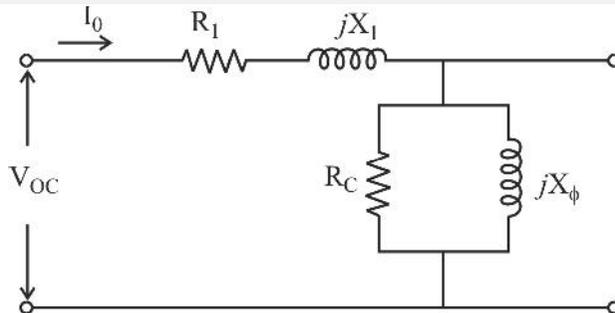
OC and SC tests on Transformer:

Open Circuit Test:



Points to Remember:

- (i) Open circuit is carried out to calculate no load loss of transformer.
- (ii) OC test is carried out with high voltage side open circuited and measuring instruments on low voltage side.
- (iii) OC test is carried out at rated voltage and frequency.
- (iv) As the HV side is open circuited, I_0 current flows in LV side which is only (at maximum) 5% of full load current, hence power measured by wattmeter can be considered to be core loss.
- (v) The circuit looks like



(vi) R_1 and X_1 can be easily neglected without much error.

(vii) The OC test is done to calculate the values of R_c and X_ϕ

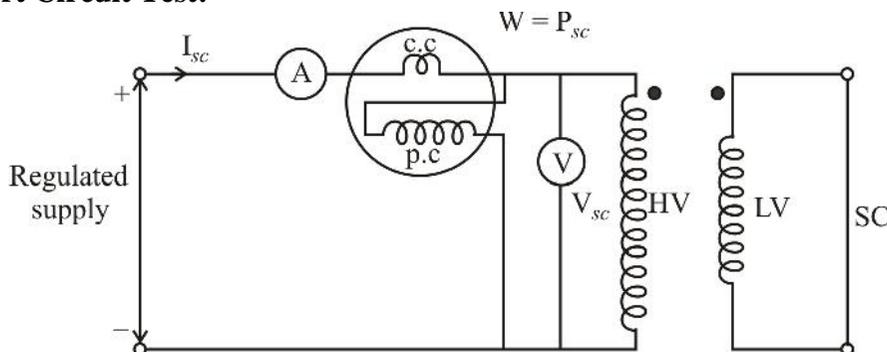
(viii) Let the wattmeter reads P_{oc} voltmeter reads V_{oc} ammeter reads I_{oc}

Then, (i) $R_c = \frac{(V_{oc})^2}{P_{oc}}$

(ii) No Load power factor angle, $\phi_o = \cos^{-1} \left(\frac{P_{oc}}{V_{oc} I_{oc}} \right)$

(iii) $X_\phi = \frac{R_c}{\tan \phi_o}$

Note: In OC test, ϕ_o is too small, hence low Pf watt-meter is used.

Short Circuit Test:

12

POWER SYSTEMS

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1. FUNDAMENTAL OF ELECTRICAL POWER SYSTEM

Work done = $F \cdot d \cos \alpha$

Where F = force applied , d = displacement, α = angle between F & d

Energy: It is capacity to do the work.

Unit : watt second $1 \text{ w - s} = 1 \text{ Joule} = 1 \text{ N - m (Newton - meters)}$

Electrical energy : It is energy that is in charged particles in an electric field.

Electrical energy generally expressed in **kilo watt hours (kwh)**

$1 \text{ kwh} = 3.6 \times 10^6 \text{ J}$

Kinetic energy (KE): $\frac{1}{2}mv^2$ (Jules)

Potential Energy (PE): Mgh (Jules)

Thermal Energy: Internal energy present in system by virtue of its temperature.

Unit : Calories $1 \text{ Cal} = 4.186 \text{ J}$

Power: it is time rate of change of energy

$$P = \frac{dw}{dt} = \frac{du}{dt} \quad u = \text{work}, \quad w = \text{energy}$$

Unit : Watt $1 \text{ Watt} = 1 \text{ J/s}$

Note: Electric motor ratings are expressed in horse power (hp)

1hp = 745.7 W and also 1 metric horse power = 735 Watt.

Electric parameter:

Let $v = \sqrt{2}V \sin \omega t$

$$i = \sqrt{2}I \sin(\omega t - \phi)$$

where v = instantaneous value voltage

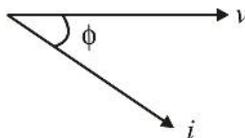
i = instantaneous value current

V = rms value of voltage

I = rms value of voltage

In Phasor representation

$$v = V \angle 0, \quad i = I \angle -\phi$$

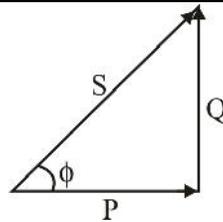


$$S = P + jQ = VI \cos \phi + jVI \sin \phi = VI^* \text{ (for this relation Q will be positive for lagging VAR)}$$

Where S = complex power or apparent power

P = Active power

Q = Reactive power

**For balanced 3 phase system**

$$P = 3 |V_p| |I_p| \cos \phi_p = \sqrt{3} |V_L| |I_L| \cos \phi_p$$

$$Q = 3 |V_p| |I_p| \sin \phi_p = \sqrt{3} |V_L| |I_L| \sin \phi_p$$

where V_L = line voltage

V_p = phase voltage

Note: in γ connection $V_p = \frac{V_L}{\sqrt{3}}$ & $I_p = I_L$

$$\Delta \text{ connection } V_p = V_L \text{ & } I_p = \frac{I_L}{\sqrt{3}}$$

Hydro power:

$$P = \rho g W h \text{ (watt)}$$

Where ρ = water density (1000 kg/m^3)

$$g = 9.81 \text{ m/s}^2$$

W = discharge rate (m^3/sec)

h = head of water

Tidal power

$$P = \rho g h^2 A/T \text{ (watt)}$$

Where h = tidal head

A = area of basin

T = period of tidal cycle

Wind power

$$P = 0.5 \rho A V^3 \text{ (watt)}$$

ρ = air density (1201 g/m^3 at NTP)

V = Wind speed in (m/s)

A = Swept area by blade (m^2)

Load Curve: It is graph between the power demands of the system w.r.t. to time.

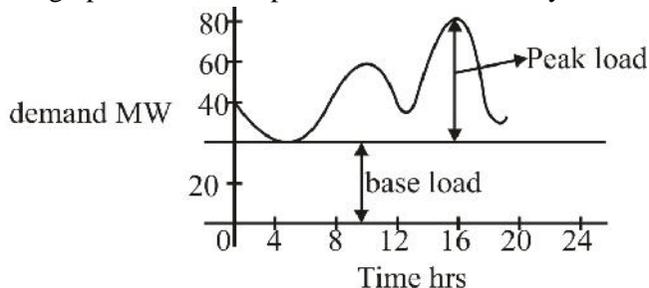


Figure: Typical daily load curve

- (i) **Base Load:** The unvarying loads which occur almost the whole day.
- (ii) **Peak load:** The various peak demands of load over and above the base load.

Designation capacity	Capital cost	Fuel cost	Typical annual load factor	Type of plant
Base load	High	Low	65-75	Nuclear, thermal
Peak load	Low	High	5-10	Gas based, small hydro, pump storage

Operational factors :

1. Demand Factor = $\frac{\text{Maximum demand}}{\text{Connected load}}$
2. Average load = $\frac{\text{energy consumed in a given period}}{\text{Hours in that time period}}$
3. Load factor = $\frac{\text{Average demand}}{\text{Maximum load}}$
4. Diversity factor = $\frac{\text{sum of individual max demands}}{\text{Maximum demand on power station}}$
5. Plant Capacity factor = $\frac{\text{Average demand}}{\text{Installed capacity}}$
6. Reserve Capacity = Plant capacity - max. demand
7. Plant use factor = $\frac{\text{Actual energy produced}}{\text{Plant capacity} \times \text{hours (the plant has been in operation)}}$

Note:

1. Load factor can be defined for a period such daily load factor, monthly load factor, annual load factor etc.
2. Practically load factor is less than 1.
3. Practically diversity factor is greater than 1.
4. Both factors should be high for economical use.

2. PER UNIT REPRESENTATION

Per unit value = $\frac{\text{the actual value in any unit}}{\text{the base value in same unit}}$

For single phase

Let Base volt amperes = $(VA)_B$

Base voltage = V_B V

Base current = $\frac{(VA)_B}{V_B}$ A

Base Impedance = $Z_B = \frac{V_B}{I_B} = \frac{V_B^2}{(VA)_B}$ ohms

$Z(pu) = \frac{Z}{Z_B} = \frac{Z(\text{ohms}) \times (VA)_B}{V_B^2}$

where $Z(\text{ohms})$ = actual Impedance

$P_{p.u} = V_{p.u} \times I_{p.u} \cos \phi$

For 3 phase

There phase base mega votamperes = $(MVA)_B$

Line to line base kilovolts = $(KV)_B$

Base current $I_B = \frac{1000 \times (MVA)_B}{\sqrt{3} \times (KV)_B}$

Base Impedance $Z_B = \frac{(KV)_B^2}{(MVA)_B}$ ohms

$P_{p.u} (3-\phi) = V_{p.u} \times I_{p.u} \cos \phi$

Change of base

$Z(Pu)_{new} = Z(Pu)_{old} \times \frac{(MVA)_{B, new}}{(MVA)_{B, old}} \times \frac{(KV)_{B, old}^2}{(KV)_{B, new}^2}$

$Z_{pu(new)} \Rightarrow$ New base value of impedance

$Z_{pu(old)} \Rightarrow$ Old base value of impedance

3. TRANSMISSION LINE

Transmission line parameter

Resistance

The effective Ac resistance

$$R_{ac} (\text{ohm}) = \frac{\text{average power loss in conductor (watts)}}{I^2}$$

Where I = Rms current (amp) in conductor

$$\text{DC resistance } R_{(DC)} = \frac{\rho l}{A} \text{ ohms}$$

ρ = resistivity of the conductor, ohm-m

l = length, m

A = Cross-sectional area, m^2

Note:

- (i) $R_{ac} = R_{dc}$ if current distribution in conductor is uniform.
- (ii) At 50Hz R_{ac} is 4% to 8% more than R_{dc} .
- (iii) Skin effect & Proximity effect both are proportional to frequency.
- (iv) The temperature dependence of resistance

$$R_2 = R_1 [1 + \alpha(T_2 - T_1)]$$

where R_2 & R_1 are the resistance at temperature T_1 and T_2 respectively

α = temp. Coefficient of resistance

Types of Conductor

AAC all-aluminium conductor

AAAC all-aluminium-alloy conductor

ACSR aluminium conductor steel reinforced

ACAR aluminium conductor, alloy-reinforced

ACSR

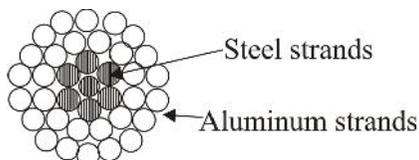


Figure: Cross-sectional view of ACSR-7 steel strands, 24 aluminium strands

$$\text{No. of strands (N)} = 3x^2 - 3x + 1$$

Where x = no. of layer

$$\text{Over all diameter of standard conductor } D = (2x - 1)d$$

where d = uniform diameter of strand

Note: In EHV (extra high voltage) expanded ACSR or bundled conductor is used.

Inductance

Single phase two wire line

$$L = 4 \times 10^{-7} \ln \frac{D}{r'} \text{ H / m}$$

Where D is distance between the centres of the conductors

$r' = re^{-1/4} = 0.7788r =$ Geometric mean radius

r = radius of conductors

Composite Conductor

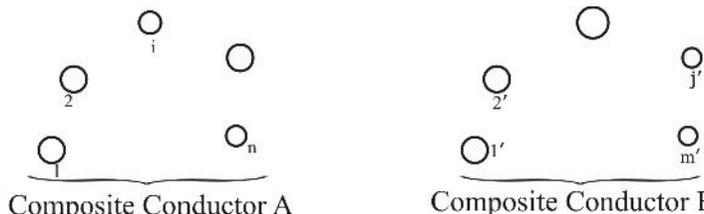


Figure: Single-phase line consisting of two composite conductors

$$L_A = 2 \times 10^{-7} \ln \frac{D_m}{D_{sA}} \text{ H / m}$$

$$L_B = 2 \times 10^{-7} \ln \frac{D_m}{D_{sB}} \text{ H / m}$$

$$L = L_A + L_B = 4 \times 10^{-7} \ln \frac{D_m}{(D_{sA} D_{sB})^{1/2}} \text{ H / m}$$

Where $D_m =$ mutual geometric mean distance

$$= \left[\prod_{i=1}^n \prod_{j=1}^{m'} D_{ij} \right]^{1/m'n}$$

$D_{sA} =$ self geometric mean distance of A

$$= \left[\prod_{i=1}^n \prod_{j=1}^n D_{ij} \right]^{1/n^2}$$

Note: Composite inductance calculation is general formula. It can be extended for bundled conductor also.

Three phase three wire line inductance

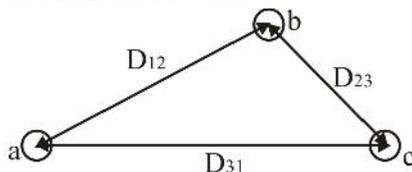
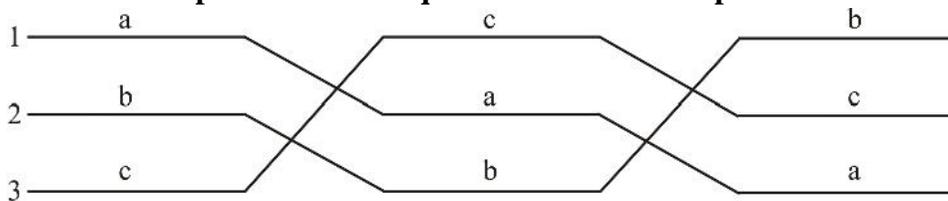


Figure: Cross-sectional view of three phase

If line are transposed to make equal inductance in all phase



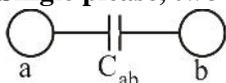
A complete transposition cycle

$$L_a = 2 \times 10^{-7} \frac{D_{eq}}{r_a^1} H / m$$

$$D_{eq} = (D_{12}D_{23}D_{31})^{1/3}$$

Capacitance:

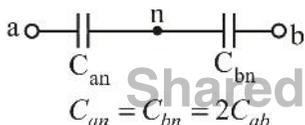
Single phase, two-wire line



(Line to line capacitance) $C_{ab} = \frac{\pi \epsilon_0}{\ln(D / r)} F / m$

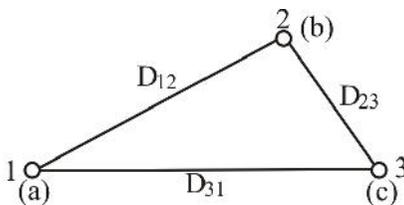
Where ϵ_0 = permittivity of free space = 8.85×10^{-12} F/m

$$C_{an} = C_{bn} = 2C_{ab}$$



(Line to neutral $C_n = \frac{2\pi \epsilon_0}{\ln(D / r)} F / m$

Three phase system



(Line to neutral) $C_{an} = \frac{2\pi \epsilon_0}{\ln(D_{eq} / r)} F / m$

Where $D_{eq} = (D_{12}D_{23}D_{31})^{1/3}$

Effect of earth on transmission line Capacitance in single phase

$$C_n = \frac{2\pi \epsilon_0}{\ln \left(\frac{D}{r \left(1 + \left(\frac{D^2}{4h^2} \right) \right)^{1/2}} \right)} F/m \text{ line to neutral}$$

Where h = distance of conductor from ground