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Code : 041302

B.Tech 3rd Semester Exam., 2014

DIGITAL ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions:

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

1. Choose the correct answer (any *seven*) : 2×7=14

(a) The binary number equivalent of decimal number 15·25 is

(i) 1111·01 *(ii)* 1010·10

(iii) 1100·01 *(iv)* 1111·10

(b) The Boolean expression

$$\overline{A}\,\overline{B}C + \overline{A}\,B\overline{C} + ABC + A\overline{B}\,\overline{C}$$

is of which gate?

(i) OR *(ii)* EX-NOR

(iii) NAND *(iv)* EX-OR

(Turn Over)

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(c) In a 4-variable K-map, a 2-variable product term is produced by

(i) a 2-cell group of 1s

(ii) an 8-cell group of 1s

(iii) a 4-cell group of 1s

(iv) a 4-cell group of 0s

(d) A feature that distinguishes the *J-K* flip-flop from the *S-R* flip-flop is the

(i) toggle condition

(ii) preset input

(iii) type of clock

(iv) clear input

(e) A full-adder can be implemented with half-adders and OR gates. A 4-bit parallel full-adder without any initial carry requires

(i) 8 half-adders and 4 OR gates

(ii) 8 half-adders and 3 OR gates

(iii) 7 half-adders and 4 OR gates

(iv) 7 half-adders and 3 OR gates

(Continued)

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(f) A modulus-12 counter must have

(i) 12 flip-flops

(ii) 3 flip-flops

(iii) 4 flip-flops

(iv) 10 flip-flops

(g) Which of the following is not a TTL circuit?

(i) 74F00

(ii) 74AS00

(iii) 74HC00

(iv) 74ALS00

(h) CMOS operates more reliably than TTL in a high-noise environment because of its

(i) lower noise margin

(ii) input capacitance

(iii) higher noise margin

(iv) smaller power dissipation

(i) The resolution of a DAC is approximately 0·4% of its full-scale range. It is

(i) 8-bit converter

(ii) 10-bit converter

(iii) 12-bit converter

(iv) 16-bit converter

(j) The number of comparators in a parallel conversion type 8-bit ADC is

(i) 8

(ii) 16

(iii) 255

(iv) 256

2. (a) Explain the operation of the following using truth table :

(i) *S-R* flip-flop

(ii) *J-K* flip-flop

(iii) *T*-type flip-flop

(b) Explain the operation of parallel in/serial out shift registers. 14

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3. (a) Sketch a NAND-NAND logic circuit for the Boolean equation $y = A\overline{B} + AC + BD$.

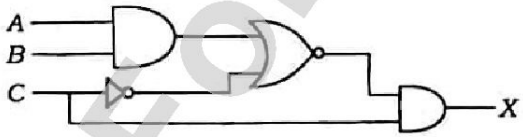
(b) (i) Simplify the following expression using Boolean algebra technique :

$$Z = (B + \overline{C})(\overline{B} + C) + \overline{\overline{A} + B + \overline{C}}$$

(ii) Show that

$$\overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C} = \overline{C}$$

(iii) Find the Boolean expression for the output of the logic circuit shown in figure below :



14

4. (a) Implement a full-adder using a decoder and two OR gates.

(b) Draw the logic diagram of an asynchronous decade counter and explain its working. 14

5. (a) Design a parity generator to generate even parity bit for a 4-bit word.

(b) Explain a 3-bit up/down synchronous counter. 14

6. Draw the circuit diagram of a monostable multivibrator using 555 timer. Explain its operation and sketch the relevant waveforms. Find the expression for the time period of the output waveform. 14

7. Implement the following Boolean function using 8 : 1 multiplexer : 14

$$f(A, B, C, D) = \Sigma m(2, 4, 5, 7, 10, 14)$$

8. Design a 4-bit full-adder with look-ahead carry generator. 14

9. Write short notes on the following : 3½×4=14

(a) CMOS

(b) EPROM

(c) Parity checker

(d) Astable multivibrators

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