Code : 041301

B.Tech 3rd Semester Exam., 2017

BASIC ELECTRONICS

Time : 3 hours *Full Marks* : 70

Instructions :

(i) The marks are indicated in the right-hand margin.

(ii) There are ***NINE*** *questions in this paper.*

(iii) Attempt ***FIVE*** *questions in all.*

(iv) Question No. ***1*** *is compulsory.*

1. Answer the following questions (any *seven*) : 2×7=14

(a) State the most important SCR parameters for high-current devices.

(b) State Fermi energy level (E_F) of an intrinsic semiconductor.

(c) Define base width modulation.

(d) Differentiate between drift current and diffusion current.

(e) Define avalanche multiplication.

(f) Define peak point current of a UJT.

(g) State the definition of threshold voltage of a MOSFET.

(h) Define CMRR of an op-amp.

(i) State the applications of photodiode.

(j) Why are PIV of bridge and centre-tapped full-wave rectifier not same?

2. *(a)* Accurately analyze the collector-to-base bias circuit is shown in figure 1 to determine the I_B, I_C and V_{CE}, when

(i) $\beta = 50$;

(ii) $\beta = 200$.

Assume $V_{BE} = 0 \cdot 7$ V.

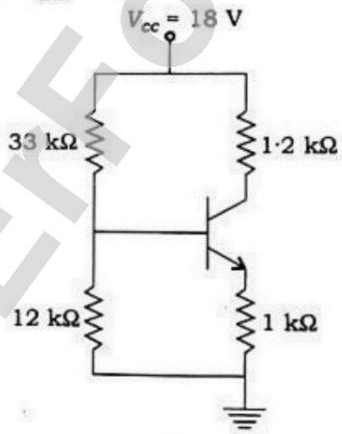

Fig. 1

(b) With the help of a neat diagram, explain the input and output characteristics of common-collector (CC) configuration. 8+6=14

3. *(a)* With the help of band and bond models, explain both *N*-type and *P*-type extrinsic silicons.

(b) A silicon *p-n* diode has a doping of $N_D = 8 \times 10^{15} cm^{-3}$ and $N_A = 2 \times 10^{16} cm^{-3}$ (for Si : $n_i = 1 \cdot 5 \times 10^{10}\ cm^{-3}$, $\varepsilon_r = 11 \cdot 9$).

(i) Determine the depletion width in the *n*-region.

(ii) Determine the built-in potential at 300 K.

(iii) Calculate the depletion width when it biased to 0·5 V. 8+6=14

4. What do you mean by rectification? Explain the working of a half-wave rectifier circuit with resistive load. With sinusoidal input, derive the expressions for the following : 4+4+4+2=14

(a) Average output voltage and current

(b) RMS load current and voltage

(c) Form factor and ripple factor

(d) Efficiency

5. *(a)* Draw the circuit of a UJT relaxation oscillator with provision for frequency adjustment and spike waveform. Show all waveforms, and explain the circuit operation.

(b) Draw the circuit diagram to show how an SCR can be triggered by the application of a pulse to gate terminal. Sketch the circuit waveforms and explain its operation. 8+6=14

6. *(a)* Explain the construction and characteristics of *n*-channel JFET.

(b) The FET circuit is shown in figure 2 has $R_1 = 3 \cdot 5\ M\Omega$, $R_2 = 1 \cdot 5\ M\Omega$, $R_s = 2\ k\Omega$, $R_L = 20\ k\Omega$, $r_d = 40\ k\Omega$ and $g_m = 2 \cdot 5$ mA/V. Find its input impedance and output impedance and voltage gain. 8+6=14

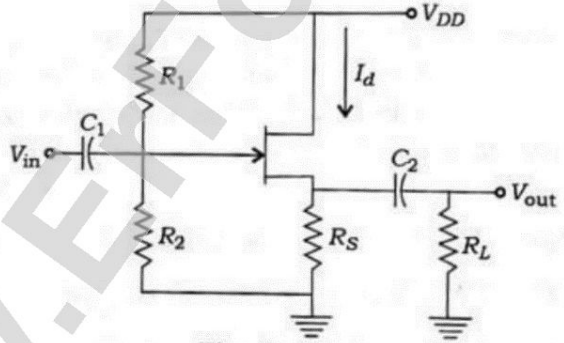

Fig. 2

7. *(a)* Given $I_E = 2 \cdot 5$ mA, $h_{fe} = 140$, $h_{oe} = 20\ \mu s$ and $h_{ob} = 0 \cdot 5\ \mu s$, determine

(i) the common-emitter hybrid equivalent circuit;

(ii) the common-base r_e-model.

(Continued)

(b) Compare the advantages and disadvantages of biasing schemes in BJT. 8+6=14

8. (a) Draw the circuit diagram of a practical voltage series feedback amplifier and derive the expressions for input resistance, output resistance, voltage gain and current gain.

(b) Explain the operation and characteristics of photodiode. 8+6=14

9. (a) Explain the summing and differential amplifiers using op-amp with derivation of output voltage.

(b) Calculate the output voltages V_2 and V_3 in the circuit of the following figure 3 :

8+6=14

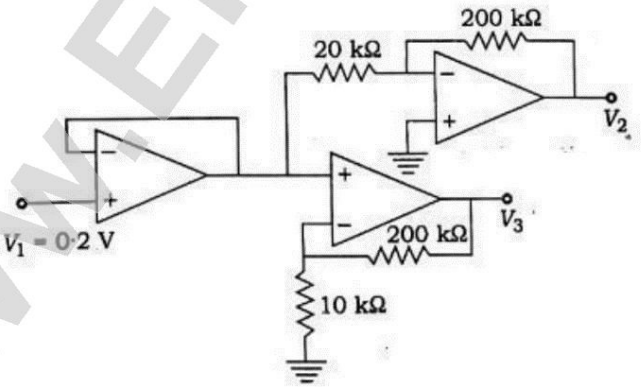

Fig. 3

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